FIG. 1

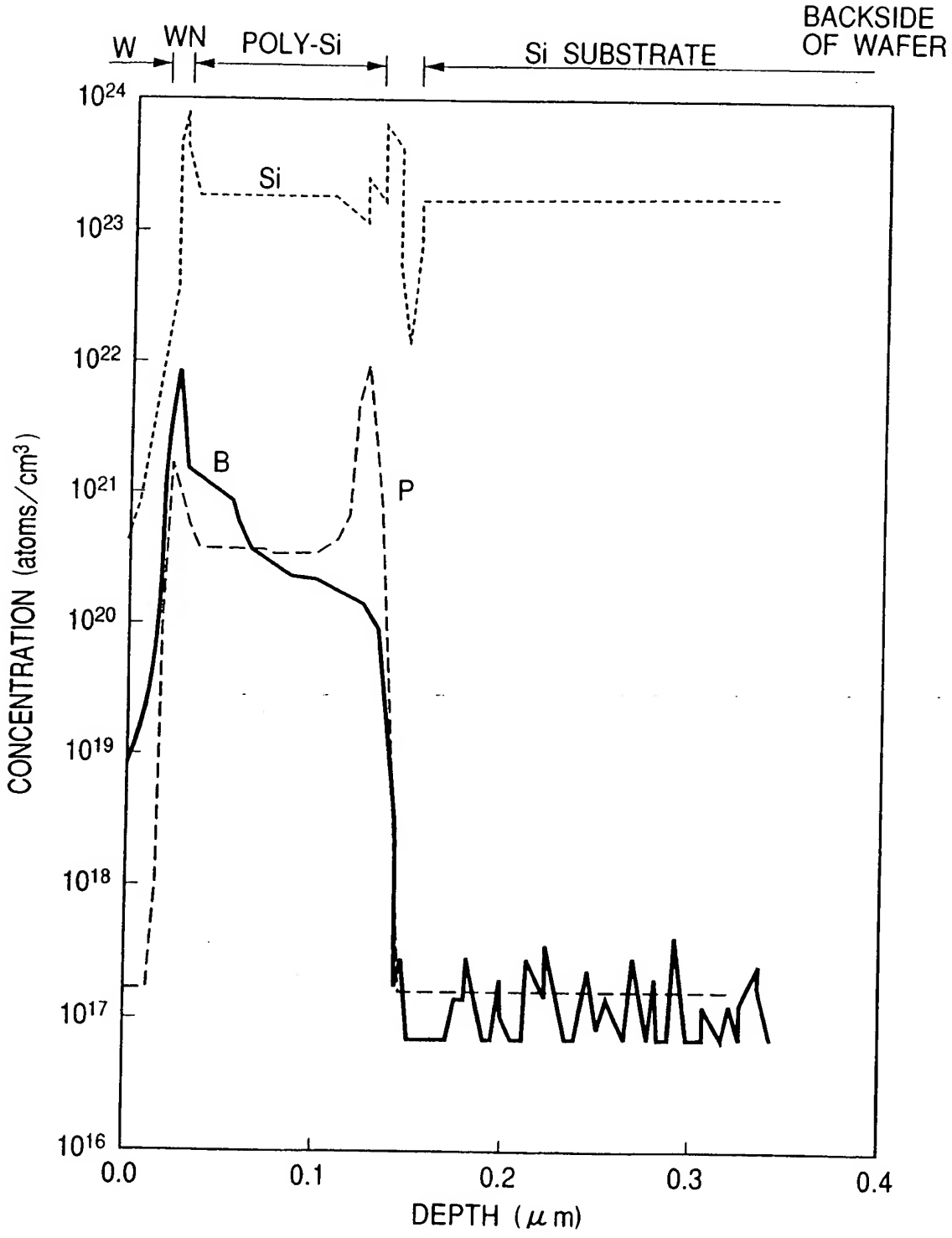

W
WN
POLY-Si
Si SUBSTRATE
BACKSIDE OF WAFER
Si
B
P
CONCENTRATION (atoms/cm³)
10²⁴
10²³
10²²
10²¹
10²⁰
10¹⁹
10¹⁸
10¹⁷
10¹⁶
0.0
0.1
0.2
0.3
0.4
DEPTH (μm)

FIG. 2A

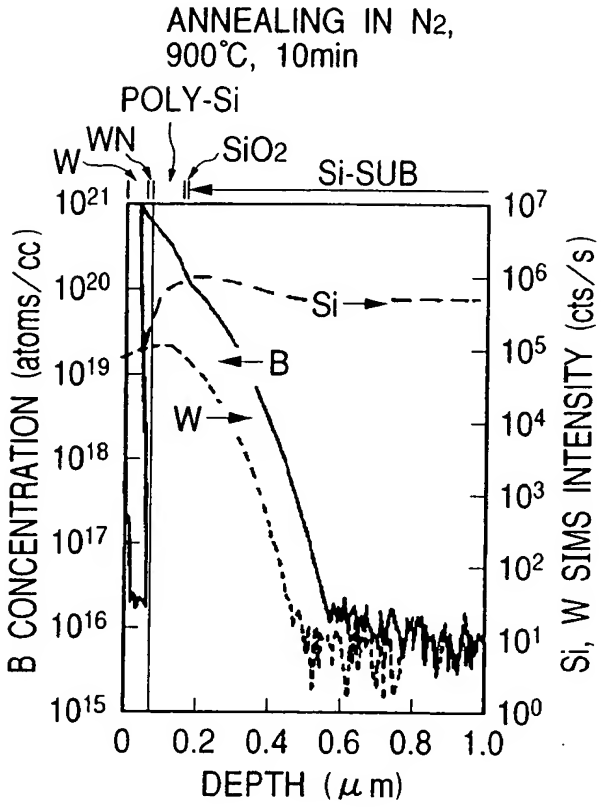


FIG. 2B

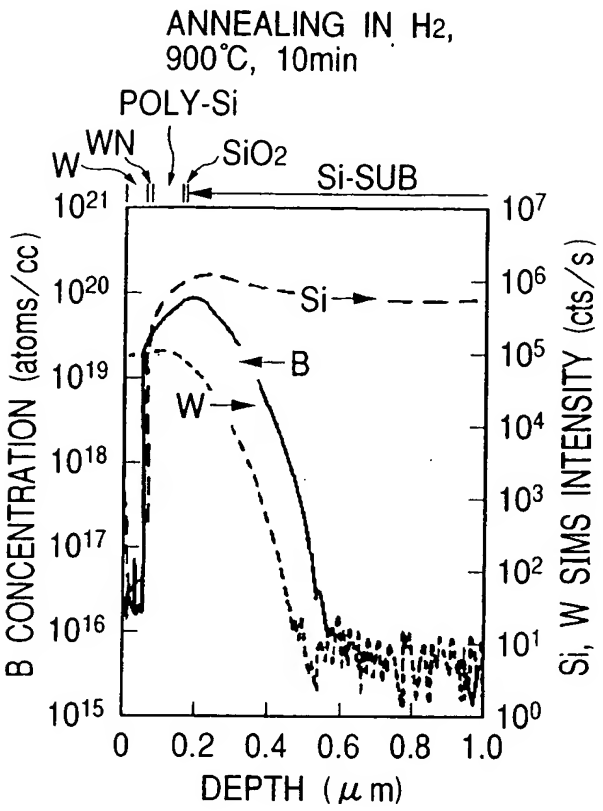


FIG. 2C

ANNEALING IN H2
WITH 5%H2O,
900℃, 10min

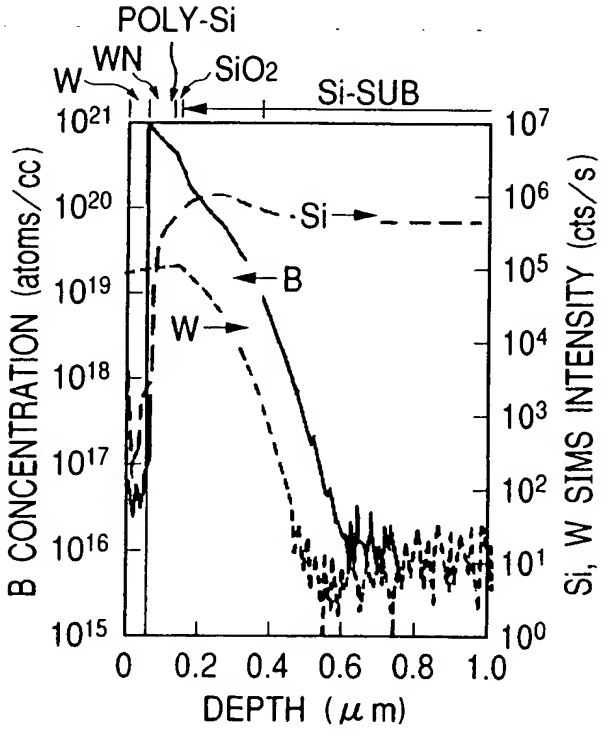


FIG. 3A

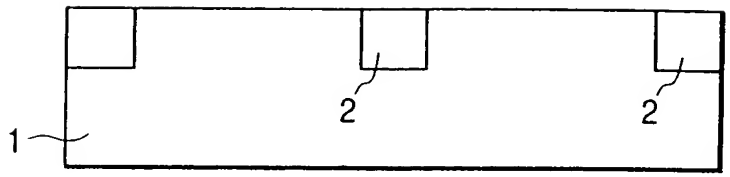


FIG. 3B

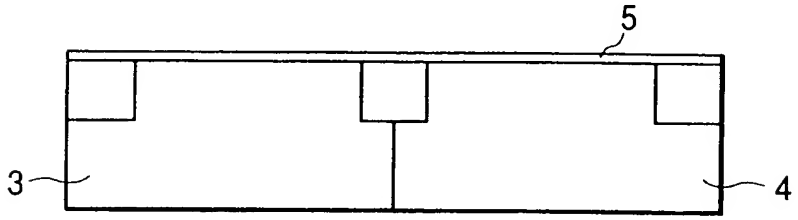


FIG. 3C

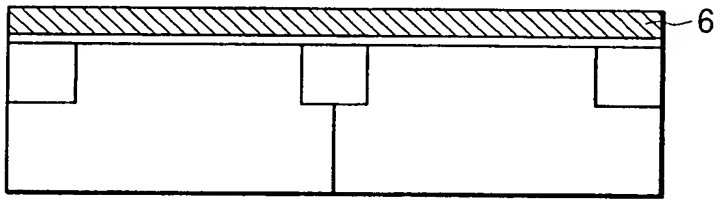


FIG. 3D

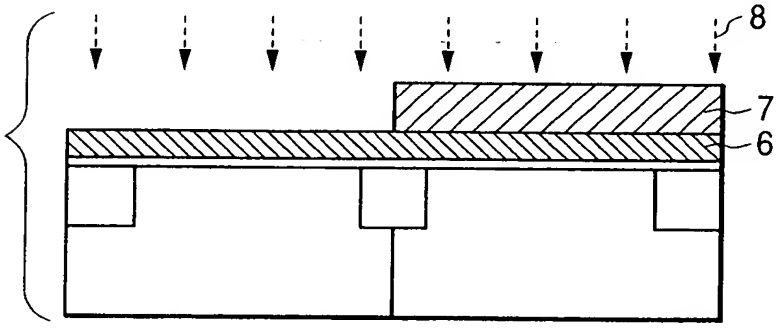


FIG. 3E

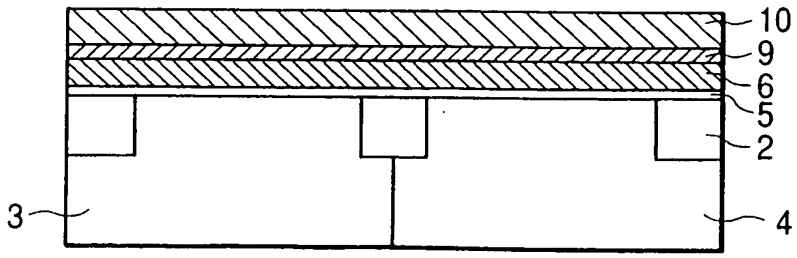


FIG. 4A

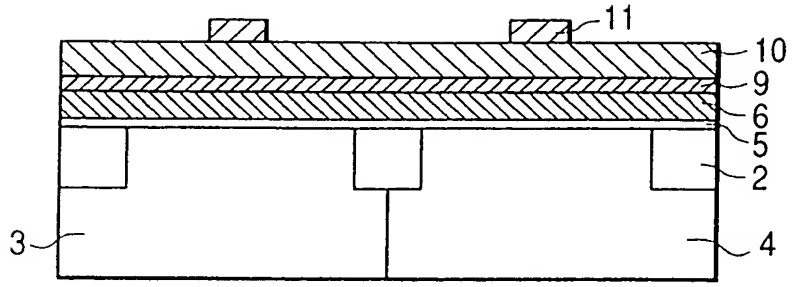


FIG. 4B

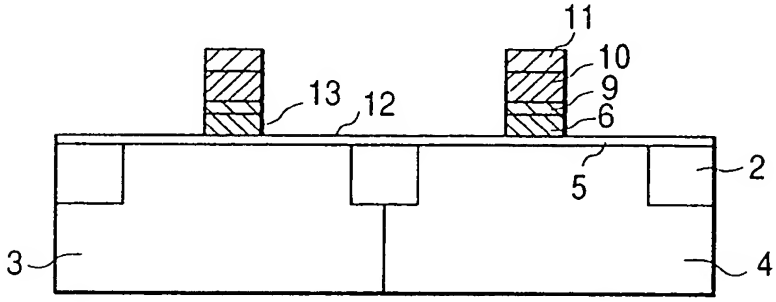


FIG. 4C

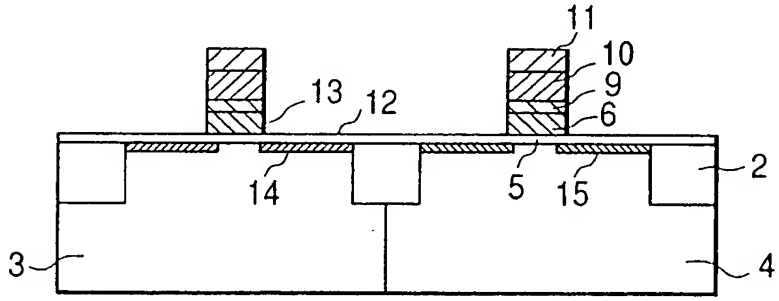


FIG. 4D

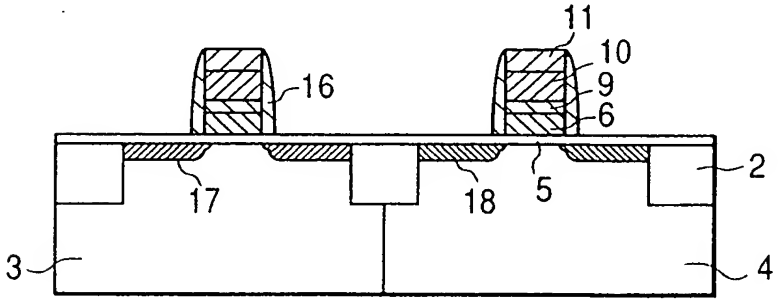


FIG. 4E

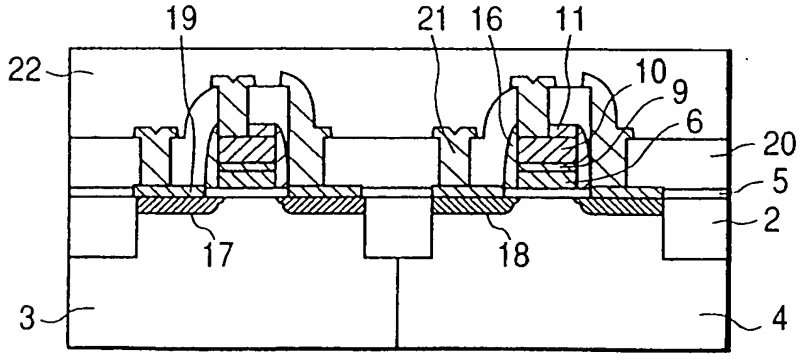
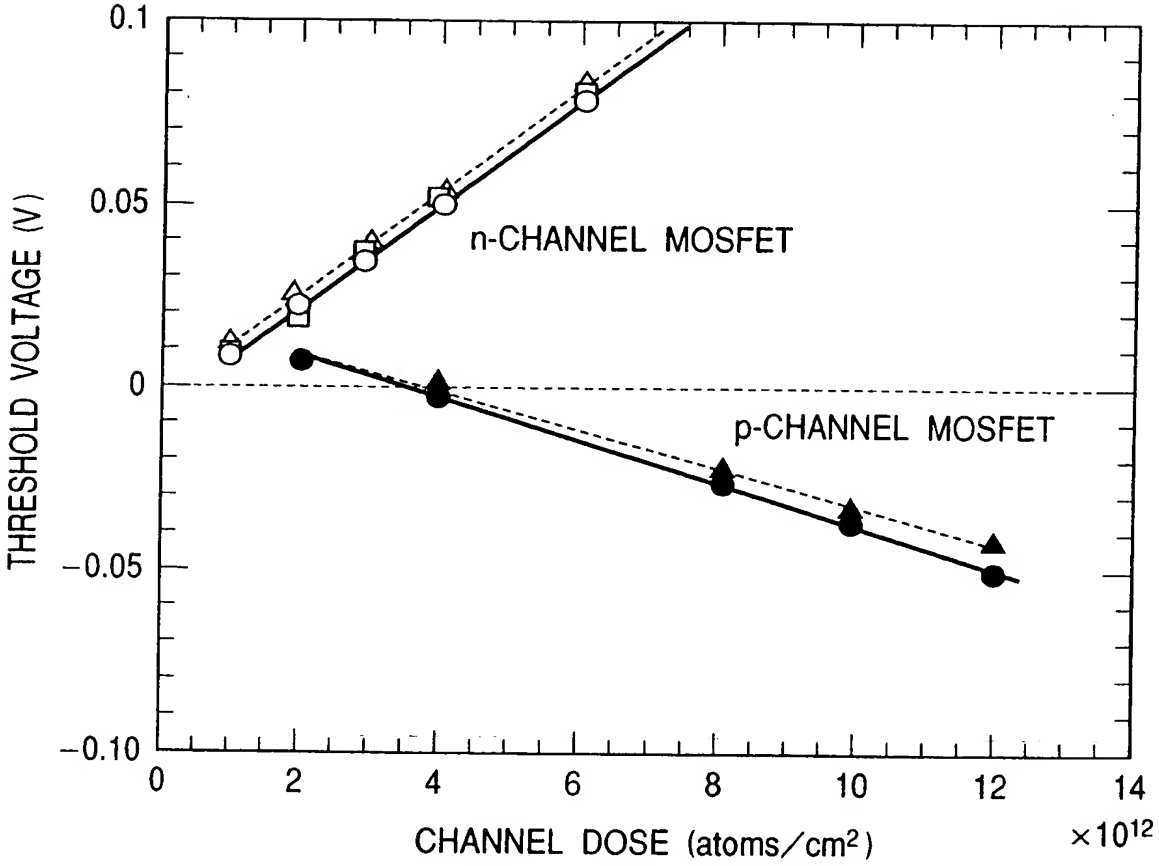


FIG. 5



W/WN/POLY-Si GATE (THIS WORK) { ● p-CHANNEL MOSFET ○ n-CHANNEL MOSFET

W/WN/POLY-Si GATE (PREVIOUS) { ▲ p-CHANNEL MOSFET △ n-CHANNEL MOSFET

POLY-Si GATE (CONVENTIONAL) □ n-CHANNEL MOSFET

FIG. 6A

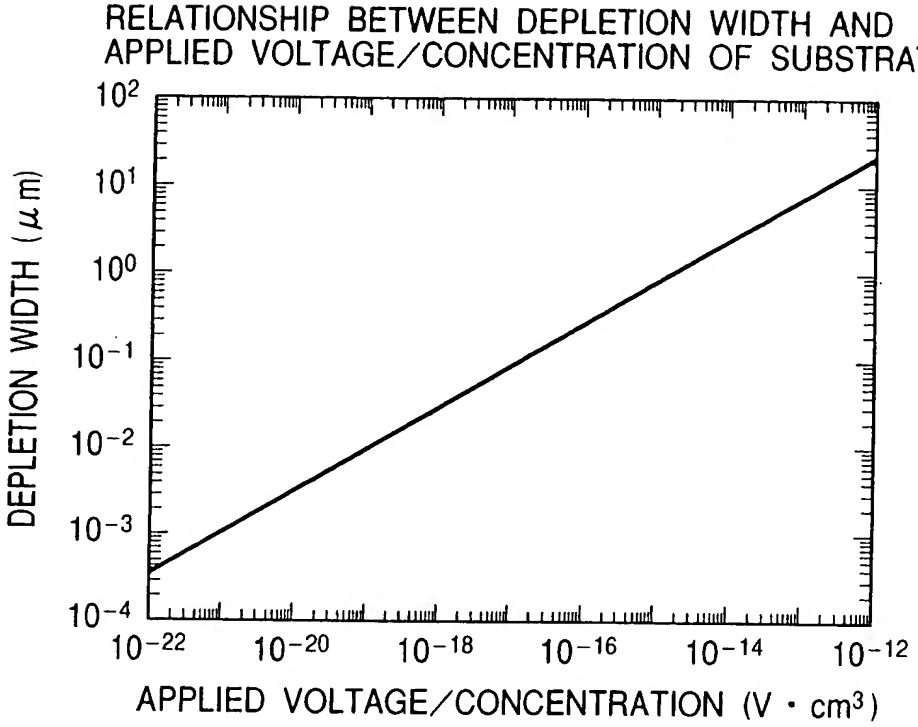

RELATIONSHIP BETWEEN DEPLETION WIDTH AND APPLIED VOLTAGE/CONCENTRATION OF SUBSTRATE
DEPLETION WIDTH (μm)
10^2
10^1
10^0
10^-1
10^-2
10^-3
10^-4
10^-22
10^-20
10^-18
10^-16
10^-14
10^-12
APPLIED VOLTAGE/CONCENTRATION (V · cm^3)

FIG. 6B

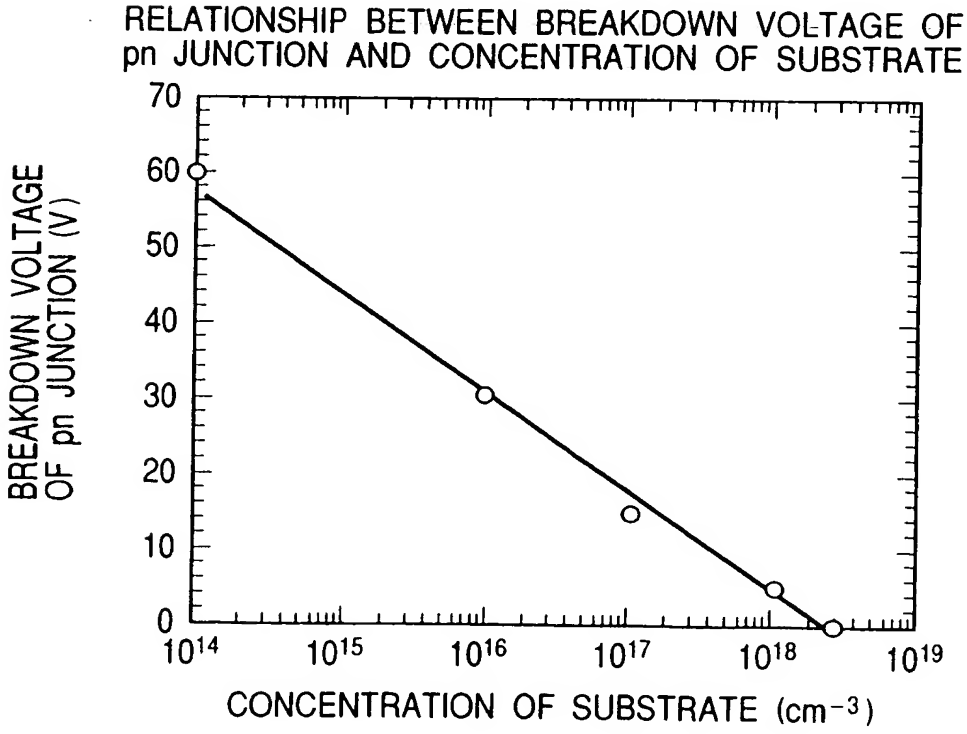
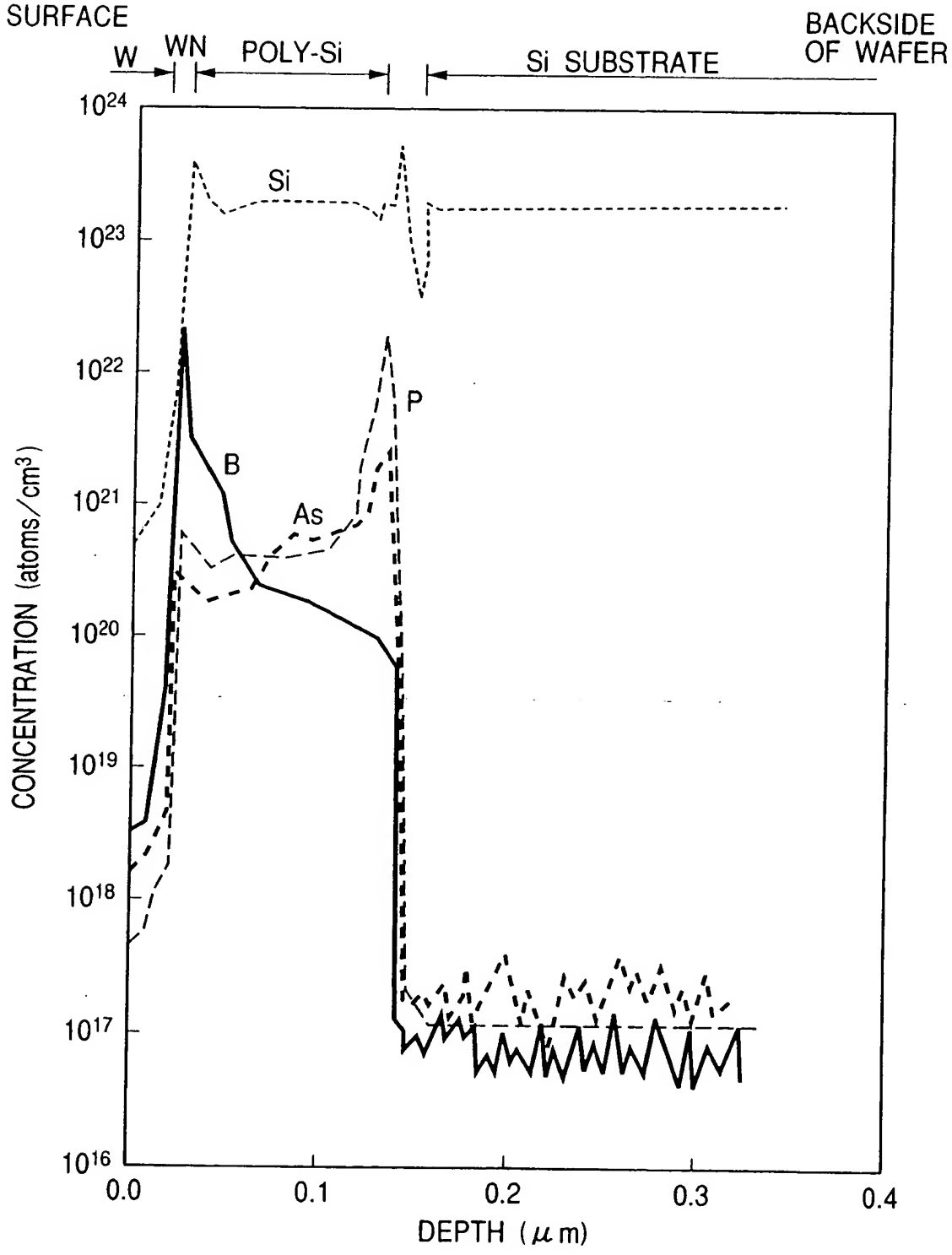

RELATIONSHIP BETWEEN BREAKDOWN VOLTAGE OF pn JUNCTION AND CONCENTRATION OF SUBSTRATE
BREAKDOWN VOLTAGE OF pn JUNCTION (V)
70
60
50
40
30
20
10
0
10^14
10^15
10^16
10^17
10^18
10^19
CONCENTRATION OF SUBSTRATE (cm^-3)

FIG. 7


SURFACE
W
WN
POLY-Si
Si SUBSTRATE
BACKSIDE OF WAFER
Si
B
As
P
CONCENTRATION (atoms/cm3)
10^24
10^23
10^22
10^21
10^20
10^19
10^18
10^17
10^16
0.0
0.1
0.2
0.3
0.4
DEPTH (μm)